## Claims

We claim:

1. A wireless communication frequency synthesizer having a phase locked loop, comprising:

a controllable oscillator;

a first clock node coupled to an output of the controllable oscillator;

a second clock node coupled to a reference clock;

a phase detector having at least a first input, a second input, and a first output, the first input being coupled to the first clock node and the second input being coupled to the second clock node; and

a sample and hold circuit coupled to the phase detector first output, the sample and hold circuit having at least one sample and hold output, the sample and hold output coupled to at least one input of the controllable oscillator.

2. A method of operating a wireless communication frequency synthesizer having a phase locked loop, comprising:

generating at least one first clock signal, the first clock signal being derived from an output clock signal of phase locked loop;

generating a second clock signal, the second clock signal being derived from a reference clock signal of phase locked loop;

detecting a phase difference between the at least one first clock signal and the second clock signal;

providing an phase difference output signal indicative of the detected phase difference;

sampling and holding the phase difference output signal at timed intervals;

generating at least one control signal from the sampling and holding step; and

controlling the output frequency of a controllable oscillator of the phase locked loop with the at least one control signal.